Distributed Active Transformer—A New Power-Combining and Impedance-Transformation Technique

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Invited Paper

***Abstract*—In this paper, we compare the performance of the newly introduced distributed active transformer (DAT) structure to that of conventional on-chip impedance-transformations methods. Their fundamental power-efficiency limitations in the design of high-power fully integrated amplifiers in standard silicon process technologies are analyzed. The DAT is demonstrated to be an efficient impedance-transformation and power-combining method, which combines several low-voltage push–pull amplifiers in series by magnetic coupling. To demonstrate the validity of the new concept, a 2.4-GHz 1.9-W 2-V fully integrated power-amplifier achieving a power-added efficiency of 41% with 50-Ω input and output matching has been fabricated using 0.35-μm CMOS transistors.**

***Index Terms*—Circular geometry, CMOS analog integrated circuit, distributed active transformer, double differential, harmonic-control, impedance transformation, low voltage, power amplifier, power combining.**

I. Introduction

AMONG THE several building blocks necessary to construct today's *holy grail* in wireless communication, the "single-chip radio," power amplifiers have been one of the most significant challenges. Several results have been published in this field, but none have reported a watt-level fully integrated power amplifier using silicon technology.

Until now, the highest output powers achieved by fully integrated power amplifiers in standard silicon processes are 85 mW [1] delivered to a differential 50-Ω load with a power-added efficiency (PAE) of 30% and 100 mW with a drain efficiency of 16% [2], both implemented in CMOS technology. Other works using CMOS [3], [4] or Si bipolar [5], [6] processes rely on the use of external passive components such as bond wire inductors, off-chip transmission lines, off-chip capacitors, and/or external baluns to achieve watt level output power.

Several other works have been reported using alternative process technologies with higher transistor breakdown voltages and/or insulating substrates to achieve watt-level output power, such as GaAs monolithic microwave integrated circuits (MMICs) [7]–[9] or silicon-on-insulator (SOI) LDMOS with 20-V breakdown voltage [10].

These results [1]–[6] demonstrate that while silicon transistors are capable of producing watt-level output power in the gigahertz-frequency range with reasonable efficiency, the on-chip passive devices are the major limiting factor in the performance of the amplifier and, therefore, deserve special attention. These passive devices are unavoidable due to the impedance transformation required to achieve high power with low-breakdown silicon transistors.

Two major problems associated with the design of on-chip power amplifiers using submicrometer CMOS processes are low transistor breakdown voltage [11] and the high loss of on-chip impedance transformation [12]. The latter is caused by the highly conductive substrate, as well as thin metal and dielectric layers. These problems become more serious as the minimum feature sizes are scaled down in each new process generation [13].

Today's submicrometer transistors necessary for gigahertz operation have breakdown voltages in the range of 4–6 V [14]. This low breakdown voltage limits the drain (collector) ac voltage swing to around ± 2 V. Without any impedance transformation, the power delivered to a 50-Ω load for a sinusoidal voltage waveform is only 40 mW. The necessary impedance transformation to achieve higher output power might be accomplished by an on-chip $1:n$ transformer or inductor–capacitor (*LC*) resonant matching network. Unfortunately, these on-chip components using CMOS processes are very lossy due to the low substrate resistivity and high metal ohmic loss [12], [15] and, therefore, they significantly degrade the output power and efficiency of the amplifier.

The distributed active transformer (DAT) is presented as an alternative method to achieve simultaneous impedance transformation and power combining that can be used to overcome

Manuscript received May 27, 2001. This work was supported by the Intel Corporation, the Army Research Office, the Jet Propulsion Laboratory, Infinion, and the National Science Foundation.

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Publisher Item Identifier S 0018-9480(02)00841-4.

the abovementioned problems [16]. This new method relies on extensive use of symmetric push–pull amplifiers, ac virtual grounds, and magnetic coupling for series power combining.

This paper presents a study of the most common passive impedance-transformation networks for watt-level fully integrated power amplifiers and compares their efficiencies to that of the DAT structure. This comparison demonstrates the advantages of the DAT approach to the existing ones. Details of the active device issues and different classes of operation will be presented in a companion paper [17]. Section II presents simple models of common transformation networks, issues related to their design, and their corresponding lowest achievable power losses. Section III explains how the DAT structure alleviates the loss in the passive components. In Section IV, the design process and measurement results of a 2.4-GHz DAT-based fully integrated power amplifier will be shown using a standard 0.35-μm CMOS transistors.

It should be noted that while this paper addresses silicon-based power amplifiers, it may also be possible to apply these techniques to other technologies such as GaAs or SOI to provide further improvements in efficiency, output power, and/or higher power density compared to conventional power amplifiers.

II. Impedance-Transformation Networks

A low loss impedance transformation with a large ratio is essential to deliver a large ac power efficiently into a 50-Ω load using low-breakdown submicrometer high-frequency integrated transistors. For instance, to deliver 2 W to a 50-Ω load using a drain voltage swing of ± 2 V, a minimum impedance-transformation ratio of 1 : 50 is necessary.

In this section, we will present an analytical study of the power efficiency of some common impedance-transformation networks as a function of their inductor unloaded quality factor $Q_{\rm ind}$ and their transformation ratio. As the quality factors of the on-chip capacitors are significantly higher than that of the inductors, their losses are not considered here.

In this paper, we will not consider conventional quarter wavelength transmission-line transformers or power-combining techniques, such as Wilkinson combiners [18], because the very high loss of the on-chip silicon transmission lines [19] makes them impractical for use in power amplifiers.

A. Resonant Impedance Transformation

LC resonant matching [18], [20], [21] is one of the most straightforward means of impedance transformation. A single *LC* section, as shown in Fig. 1, may be used to perform impedance matching. In some cases, it may be desirable to cascade several such sections to enhance the efficiency. We will analyze the single section and extend the analysis to the general multisection case.

Using the single section network in Fig. 1, an impedance-transformation ratio r is achieved with a parallel inductor and a series capacitor. The dual network with a parallel capacitor and a series inductor may also be used. However, a series capacitor has the added advantage of blocking the dc current from flowing through the load, and a parallel inductor with a terminal connected to ground lowers the energy coupling into the substrate

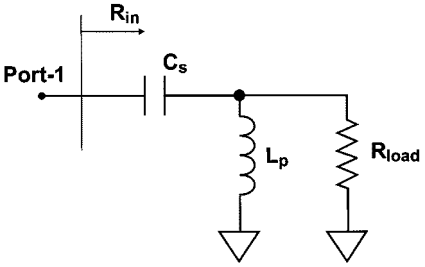


Fig. 1. Ideal resonant *LC* impedance-transformation network.

and hence lowers the associated loss of the inductor. The dual network, however, results in better harmonic suppression due to its low-pass nature.

The impedance-transformation ratio r is defined as

$$r \equiv \frac{R_{\rm load}}{R_{\rm in}} = 1 + Q_l^2 \approx Q_l^2 \tag{1}$$

where $R_{\rm load}$ and $R_{\rm in}$ are the load and its transformed impedance at port-1, and Q_l is the loaded quality factor of the network at the angular frequency, ω, assuming lossless passive components, i.e.,

$$Q_l = \frac{R_{\rm load}}{\omega L_p}. \tag{2}$$

The voltage swing limitations of the active device in combination with desired output power determine $R_{\rm in}$. A given $R_{\rm in}$ and $R_{\rm load}$ will set r and Q_l in (1). Then (2) can be used to calculate the value of the inductor, L_p. Knowing L_p, the capacitor value can be selected using the following resonant condition:

$$\frac{1}{\omega C_s} = \frac{\omega L_p}{1 + \dfrac{1}{(R_{\rm load}/\omega L_p)^2}} = \frac{\omega L_p}{1 + \dfrac{1}{Q_l^2}} \approx \omega L_p. \tag{3}$$

While complete models for on-chip inductors have been devised [22], the loss of a one-port inductor L_P at a single frequency can always be modeled using a single parallel resistor R_{lp} or by using its unloaded quality factor $Q_{\rm ind}$ defined as

$$Q_{\rm ind} = \frac{R_{lp}}{\omega L_p} \tag{4}$$

at the frequency of interest. Fig. 2 shows the resonant impedance-transformation network with the simplified narrow-band inductor model. The passive power transfer efficiency η of this network, calculated as the ratio between the input RF power and the RF power delivered to the load can be computed as a function of $Q_{\rm ind}$, and r as follows:

$$\begin{aligned} \eta &\equiv \frac{P_{\rm out}}{P_{\rm in}} \\ &= \frac{|V_l|^2/(2R_{\rm load})}{|V_l|^2/(2(R_{\rm load}\|R_{lp}))} \\ &= \frac{1/R_{\rm load}}{1/R_{lp} + 1/R_{\rm load}} \\ &= \frac{1}{1 + \dfrac{R_{\rm load}}{\omega L_p Q_{\rm ind}}}. \end{aligned} \tag{5}$$

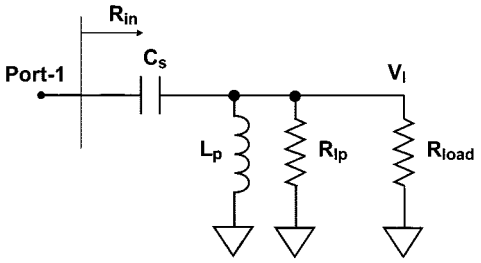


Fig. 2. Resonant *LC* impedance-transformation network with loss.

The efficiency is the ratio between the load conductance, $1/R_{\rm load}$, and total conductance, $1/R_{lp} + 1/R_{\rm load}$. The impedance-transformation ratio r in the presence of loss can be easily calculated using (1) as a function of R_{lp}, $R_{\rm load}$, unloaded inductor $Q_{\rm ind}$, and total loaded quality factor $Q_{\rm total}$, namely,

$$r = \frac{R_{\rm load}}{\left(\dfrac{R_{\rm load}\|R_{lp}}{1+Q_{\rm total}^2}\right)} = \frac{\left(1+\dfrac{R_{\rm load}}{R_{lp}}\right)^2 + Q_{\rm ind}^2\left(\dfrac{R_{\rm load}}{R_{lp}}\right)^2}{1+\dfrac{R_{\rm load}}{R_{lp}}} \tag{6}$$

where the total loaded quality factor $Q_{\rm total}$ is defined as

$$Q_{\rm total} = \frac{R_{\rm load}\|R_{lp}}{\omega L_p}. \tag{7}$$

Equations (4) and (6) can be solved for ωL_p in terms of the desired transformation ratio r, load resistance $R_{\rm load}$, and inductor quality factor $Q_{\rm ind}$, i.e.,

$$\omega \cdot L_p = \frac{R_{lp}}{Q_{\rm ind}} = \frac{2(Q_{\rm ind}+1/Q_{\rm ind})}{r-2+\sqrt{r^2+4Q_{\rm ind}^2(r-1)}} \cdot R_{\rm load} \tag{8}$$

which can be used to calculate the value of L_p in the design process. In practice, $Q_{\rm ind}$ and r are both functions of L_p and, therefore, several iterations may be necessary to obtain the exact value of L_p.

The efficiency of the transformation network η can also be calculated as a function of $Q_{\rm ind}$ and r from (5) and (8)

$$\eta = \frac{Q_{\rm ind}^2+1}{Q_{\rm ind}^2+\dfrac{r+\sqrt{r^2+4Q_{\rm ind}^2(r-1)}}{2}} \approx \frac{1}{1+\dfrac{r}{Q_{\rm ind}^2}}. \tag{9}$$

For any matching network, we can define the power enhancement ratio (PER) E as the ratio of the RF power delivered to the load with a transformation network in place $P_{\rm trans}$ to the power delivered to the load for the same sinusoidal input voltage source when it drives the load directly $P_{\rm direct}$, i.e.,

$$E \equiv \frac{P_{\rm trans}}{P_{\rm direct}} = \frac{P_{\rm direct}\cdot r\cdot \eta}{P_{\rm direct}} = r\cdot\eta. \tag{10}$$

Unlike r, PER accounts for the loss in the passive impedance-transformation ratio and is thus particularly important for lossy on-chip passive components in silicon technology.

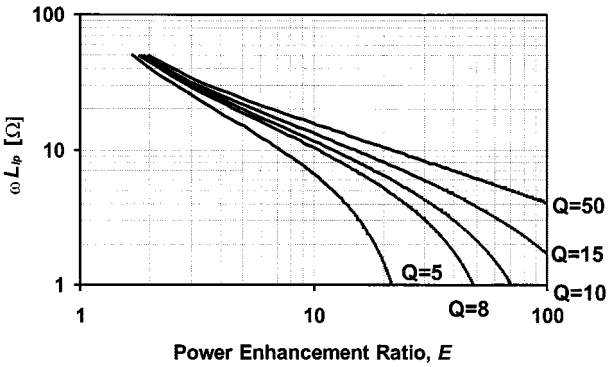


Fig. 3. Required inductor reactance versus PER and inductor Q for a resonant impedance-transformation network.

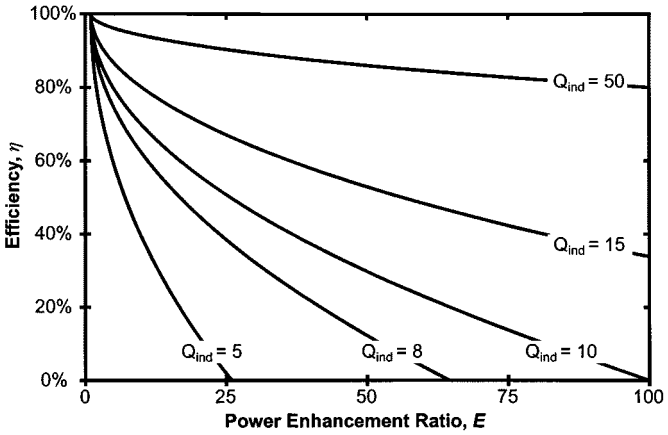


Fig. 4. Efficiency versus PER and inductor Q for a single section resonant impedance-transformation network.

Using the definition in (10) together with (4)–(6), we can find a closed-form solution to calculate the passive network efficiency η for a necessary E and available inductor $Q_{\rm ind}$, as follows:

$$\eta = 1 - \frac{\sqrt{E-1}}{Q_{\rm ind}} \approx 1 - \frac{\sqrt{E}}{Q_{\rm ind}}. \tag{11}$$

Furthermore, ωL_p can be calculated from E and $Q_{\rm ind}$ as follows:

$$\omega \cdot L_p = \frac{R_{lp}}{Q_{\rm ind}} = \left(\frac{1}{\sqrt{E-1}} - \frac{1}{Q_{\rm ind}}\right) R_{\rm load}. \tag{12}$$

Appendix A contains the derivations leading to (11) and (12).

Fig. 3 shows plots of ωL_p versus E for several different values of $Q_{\rm ind}$ and a 50-Ω load resistor $R_{\rm load}$ for a single *LC* section. As can be seen from these graphs, for a PER of 50, a reactance of $2j\Omega$ is necessary if an inductor with $Q_{\rm ind}$ of ten is to be used.

Fig. 4 shows plots of η versus E for several different $Q_{\rm ind}$ for a single section network. For instance, with a PER of 50 and an inductor $Q_{\rm ind}$ of ten, the matching network *alone* will have a maximum passive power efficiency of around 30%. This does not include any loss in the active device, the driving network, or the external connections. We can also see in the Fig. 4 that, for a given inductor quality factor $Q_{\rm ind}$, there is an upper bound

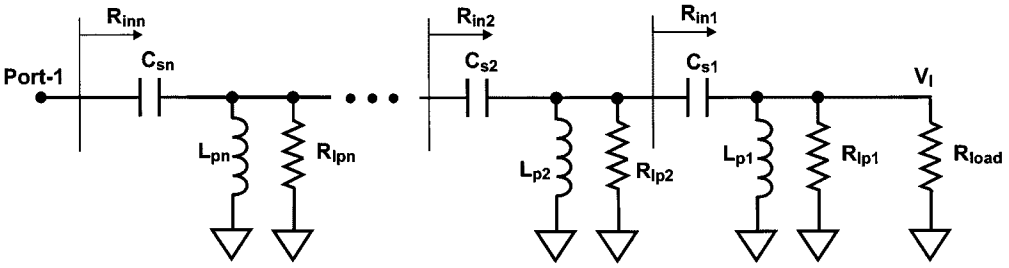


Fig. 5. Multisection resonant *LC* impedance-transformation network with loss.

on the maximum achievable PER E, where the efficiency η becomes zero. This maximum achievable PER E_{MAX} can be calculated from (11) to be

$$E_{\mathrm{MAX}} = 1 + Q_{\mathrm{ind}}^2. \tag{13}$$

Equation (13) provides an upper bound on the value of E in a single inductor–capacitor section. However, it should be noted that the efficiency would drop to zero as we approach this E_{MAX}, making this bound unachievable.

A similar analysis can be performed for the more general case of multisection transformation with n segments, as shown in Fig. 5. Assuming the same load enhancement ratio $E^{1/n}$ for each individual section to have an overall PER E, the derivations in Appendix A leads to the following expression for passive efficiency:

$$\eta = \left(1 - \frac{\sqrt{E^{1/n} - 1}}{Q_{\mathrm{ind}}}\right)^n. \tag{14}$$

The inductance value for the kth parallel inductor $L_{p,k}$ in the chain can be calculated as follows:

$$\omega \cdot L_{p,k} = \left(\frac{1}{\sqrt{E^{1/n} - 1}} - \frac{1}{Q_{\mathrm{ind}}}\right) \cdot \left(\frac{1 - \dfrac{\sqrt{E^{1/n} - 1}}{Q_{\mathrm{ind}}}}{E^{1/n}}\right)^{k-1} \cdot R_{\mathrm{load}}. \tag{15}$$

In principle, the multisection transformation network has a lower loss for high PER compared to a single section. However, it requires a more complex layout and some of its inductors will have very large or very small reactance compared to a single section. This results in a lower overall quality factors Q for the network. Fig. 6 shows plots of η versus E for several different values of Q_{ind} for a multisection network. This figure only shows the efficiencies η for the number of sections leading to the minimum loss, so it can also be used to find the optimum number of sections. For example, we can see that with a PER of 50 and an inductor quality factor Q_{ind} of ten, the best matching network will have three *LC* sections and will have a maximum passive efficiency of around 60%. Again, this figure does not include any loss in the active device, the dc feeds, or the external connections.

Equations (11) and (12) have important implications regarding the necessary reactance, transformation efficiency, and the PER. In particular, (12) suggests that the inductor reactance necessary for this type of matching network with a single

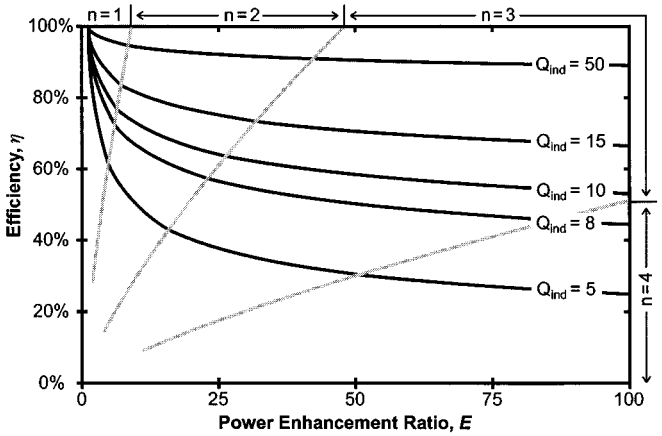


Fig. 6. Efficiency versus PER and inductor Q for a multisection resonant network. Vertical gray lines separate regions using different number of sections. The best number of sections n from 1–4 is chosen for the highest efficiency for different PERs and inductor Q.

section decreases rapidly as the desired PER E is increased as seen in Fig. 3. More importantly, the transformation efficiency η also decreases quickly with higher PER E, as can be seen in Fig. 4. In a multisection approach, the loss is improved significantly compared to the single-section network, but still increases with higher PER E, as can be seen from Fig. 6. This analysis provides the theory for what PA designers have long understood by intuition and experience. The low Q passives currently available on chip fundamentally limit achievable power efficiencies at the 1-W level. No amount of complexity in an *LC* transformation network can overcome this.

B. Magnetically Coupled Transformer Impedance Transformation

By magnetically coupling two inductors, we can create a coupled-inductor transformer. In a coupled-inductor transformer, the magnetic field created by the port-1 current I_1 through the primary inductor L_1 generates a voltage in the secondary inductor L_2. At the same time, the current through the secondary I_2 will magnetically induce a voltage in the primary circuit. The port voltages of the loosely coupled lossy transformer V_1 and V_2 in Fig. 7(a) are related to its port currents through

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -R_2 - j\omega L_2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{16}$$

$$M = k \cdot \sqrt{L_1 \cdot L_2}$$

$$n = \sqrt{\frac{L_2}{L_1}} \approx \frac{I_1}{I_2} \approx \frac{V_2}{V_1}$$

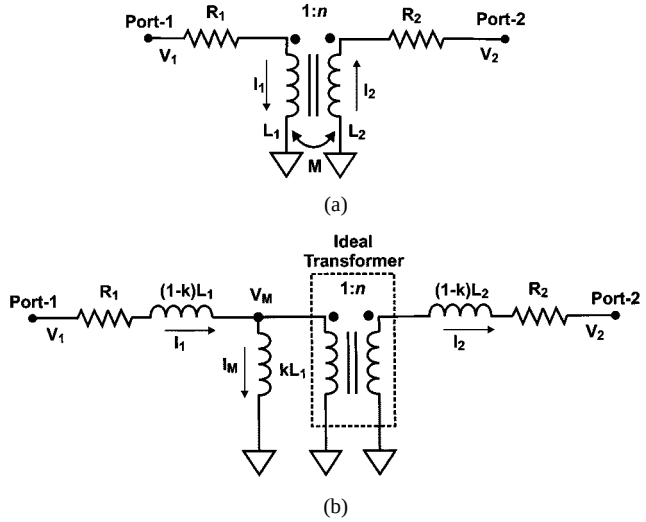


Fig. 7. (a) Transformer model. (b) Transformer equivalent T-model.

where M is the mutual inductance, k is the coupling factor, r is the transformation ratio, and n is the turn ratio between primary and secondary coils. Fig. 7(b) shows the equivalent model for the transformer of Fig. 7(a), where the lossy inductors of the transformer are modeled by the equivalent series resistors R_1 and R_2 and net inductances L_1 and L_2 for a single frequency [23]. The quality factors Q_1 and Q_2, of the primary and the secondary inductors can be calculated in terms of R_1 and R_2, respectively, i.e.,

$$Q_1 = \omega L_1/R_1 \quad Q_2 = \omega L_2/R_2. \tag{17}$$

The quality factors of the coupled inductors are slightly different from those of the individual inductors due to the current redistribution that occurs on both inductors when they are coupled. This effect is shown in the current density graph of Fig. 8, which shows the current densities in stand alone primary and secondary loops as well as the redistributed current densities due to their magnetic coupling. These graphs were obtained using the Sonnet electromagnetic simulator [24].

The leakage inductances $(1-k)L_1$ and $(1-k)L_2$ can have a significant effect on the primary and secondary reactance if the coupling factor k is small. The factor k is low for on-chip spiral transformers because of the low permeability of the core material (e.g., SiO_2) and the planar geometry that results in large magnetic field leakage.

If the transformer is used to achieve output matching in a power amplifier, it will be necessary to resonate some of the transformer's inductance to minimize the loss. This effect is discussed in more detail in Appendix B. A capacitor is also necessary on the primary side of the transformer to adjust its input reactance to the desired value for the driving transistor. This can be done using a parallel capacitor on the primary and another capacitor in series with the secondary, as shown in Fig. 9(a), and its expanded form using the equivalent T-model in Fig. 9(b).

Now, we can use the equivalent model of Fig. 9(b) to calculate the transformer efficiency η, the best value of the series matching capacitor C_l, and the best inductor values L_1 and L_2 for the lowest loss as a function of the load resistance R_l and other transformer characteristics.

The transformer efficiency η is the ratio of power delivered to the load P_{load} to the total power delivered into port-1 of the network P_{total}, which is calculated in Appendix B to be

$$\eta \equiv \frac{P_{\text{load}}}{P_{\text{total}}} = \frac{R_l/n^2}{\left(\dfrac{\omega L_1/Q_2 + R_l/n^2}{\omega k L_1}\right)^2 \cdot \dfrac{\omega L_1}{Q_1} + \dfrac{\omega L_1}{Q_2} + R_l/n^2}. \tag{18}$$

This η is obtained assuming $L_1 \cong L_2/n^2$ and using the optimum value of C_l given by

$$\frac{1}{\omega C_l} = \omega L_2. \tag{19}$$

Equation (18) can be differentiated to obtain the optimum value of L resulting in the highest possible η, which is

$$\omega L_1 = \frac{R_l}{n^2\sqrt{\dfrac{1}{Q_2^2} + \dfrac{Q_1}{Q_2}\cdot k^2}} = \frac{A \cdot R_l}{n^2} \tag{20}$$

where

$$A \equiv \frac{1}{\sqrt{\dfrac{1}{Q_2^2} + \dfrac{Q_1}{Q_2}\cdot k^2}}. \tag{21}$$

Using this optimum L_1, the maximum efficiency will be given by

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \dfrac{1}{Q_1 Q_2 k^2}\right)\dfrac{1}{Q_1 Q_2 k^2}} + \dfrac{2}{Q_1 Q_2 k^2}}. \tag{22}$$

The above equation shows that passive efficiency η can be maximized using a k as close as possible to unity. This is because the smaller the k, the larger fraction of the primary inductor current I_1 will go through the magnetizing inductor kL_1 and, hence, a lower power will be delivered to the load resistor. More importantly, unlike resonant matching, the transformer efficiency is not affected by the transformation ratio, as seen in (22).[1] Fig. 10 shows how the transformer efficiency is reduced when the reactance of the inductor is above or below the optimum value determined by (20). Several plots of η versus ωL_1 are shown for a 50-Ω load and a peak PER E of 50. For each plot, a fixed r is used in order to have PER $= 50$ for peak η. In these plots, Q_1 and Q_2 are assumed to be equal to facilitate visualization.

The equivalent input admittance of the transformer for the optimum values of C_l and L_1 given by (19) and (20) can be calculated to be

$$Y_{\text{in}} \equiv \frac{1}{Z_{\text{in}}} = G_{\text{in}} + jB_{\text{in}} \approx \frac{Q_1}{\dfrac{Q_1}{k^2} + Q_2}\left(\frac{n^2}{R_l} + j\frac{1}{\omega L_1}\right). \tag{23}$$

[1]Except to the degree that L_1, L_2, k, Q_1, and Q_2, change with r.

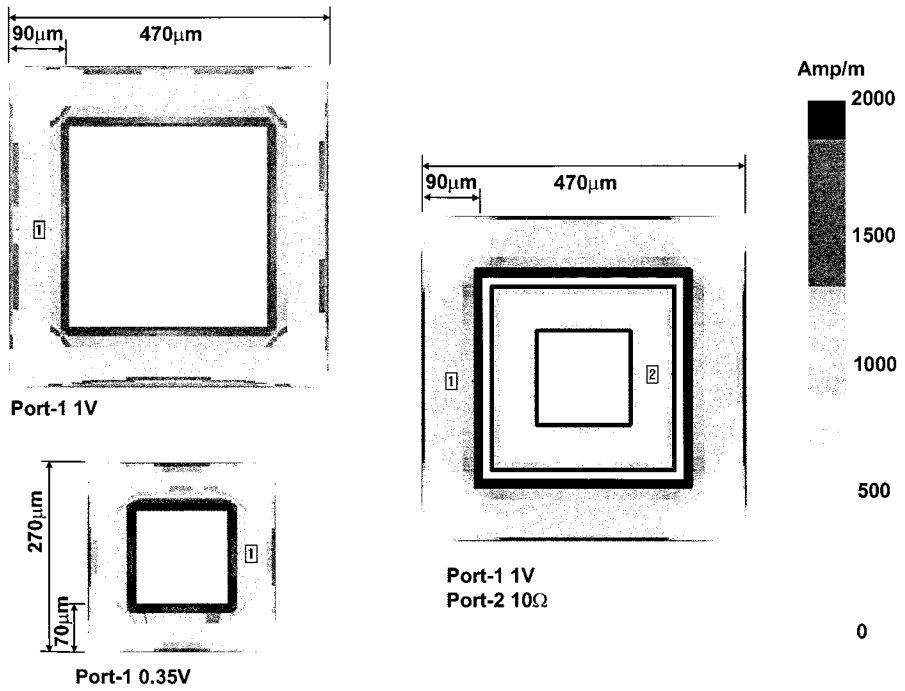


Fig. 8. Current densities in planar one turn inductors and a planar transformer.

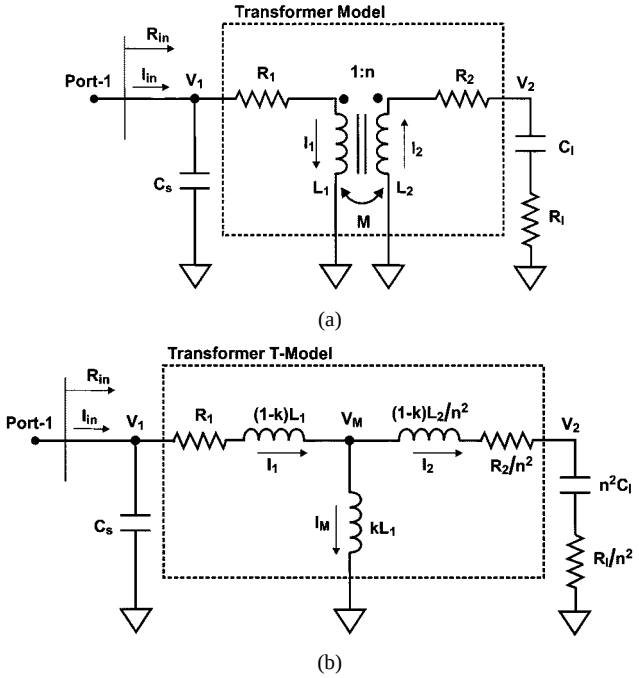


Fig. 9. (a) Transformer model with load and tuning capacitors. (b) Transformer equivalent T-model with load and tuning capacitors.

We now calculate the transformer turn ratio n for a desired PER E using (10) and (23) using the assumption $k^2Q_1Q_2 \gg 1$

$$E = \eta \frac{R_l}{(1/G_{\text{in}})} \approx \eta \frac{n^2 Q_1}{\left(\frac{Q_1}{k^2} + Q_2\right)} \tag{24}$$

$$n \approx \sqrt{\frac{E(Q_1/k^2 + Q_2)}{\eta Q_1}}. \tag{25}$$

Fig. 11 shows plots of η versus Q_1 and Q_2 for $k = 0.4, 0.6, 0.8$, and 1 using (22). As an example, to obtain a transformation ratio of 50 with primary and secondary inductor quality factors of ten and a k of 0.6, the transformer primary circuit should have an impedance of approximately $1j\Omega$ at the frequency of operation to achieve the highest efficiency. In this case, n should be approximately eight and the best achievable passive efficiency is 70%.

Although a single series capacitor with the load can provide the necessary negative reactance to resonate the inductive output of the transformer, an additional capacitor C_{out} parallel to the load (Fig. 12) can be used to adjust the real part of the impedance seen by the secondary of the transformer to lower its loss. This extra degree of freedom can be used to obtain a lower turn ratio n and a lower primary inductance L_2 for a given load resistance and PER E.

Equations (22), (24), and (25) determine the optimum value of η and the resultant E and n for $C_{\text{out}} = 0$. We can recalculate these parameters for the other limiting case, when C_l is large ($C_l = \infty$), using (10), (16), (19), (20), and (24). The new PER E is

$$E \approx (1 + A^2) \cdot \eta \frac{n^2 Q_1}{\left(\frac{Q_1}{k^2} + Q_2\right)} \tag{26}$$

which is obtained for a C_{out} and an L_1 given by

$$\frac{1}{\omega C_{\text{out}}} = \frac{AR_l}{1 + A^2}$$
$$\omega L_1 = \frac{1}{(1 + A^2)} \frac{AR_l}{n^2}. \tag{27}$$

The new input admittance is

$$Y_{\text{in}} \approx \frac{1}{1 + A^2} \cdot \frac{Q_1}{\frac{Q_1}{k^2} + Q_2} \cdot \left(\frac{n^2}{R_l} + j\frac{1}{\omega L_1}\right). \tag{28}$$

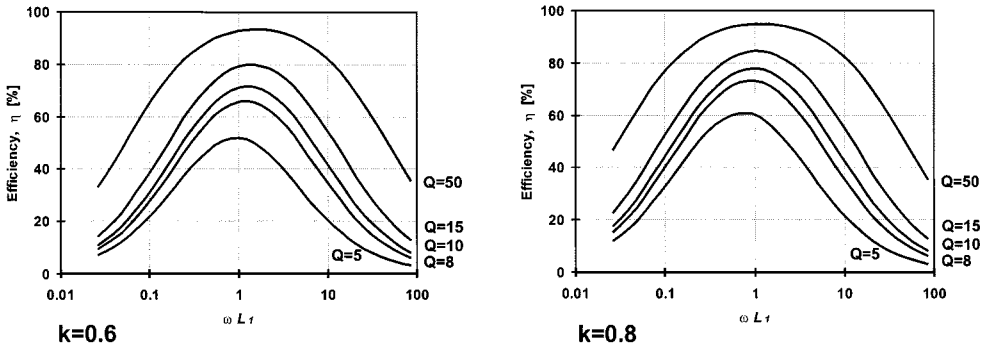


Fig. 10. Efficiency versus primary inductor reactance normalized to load resistance, inductor Q, and coupling factor k for a transformer with loss.

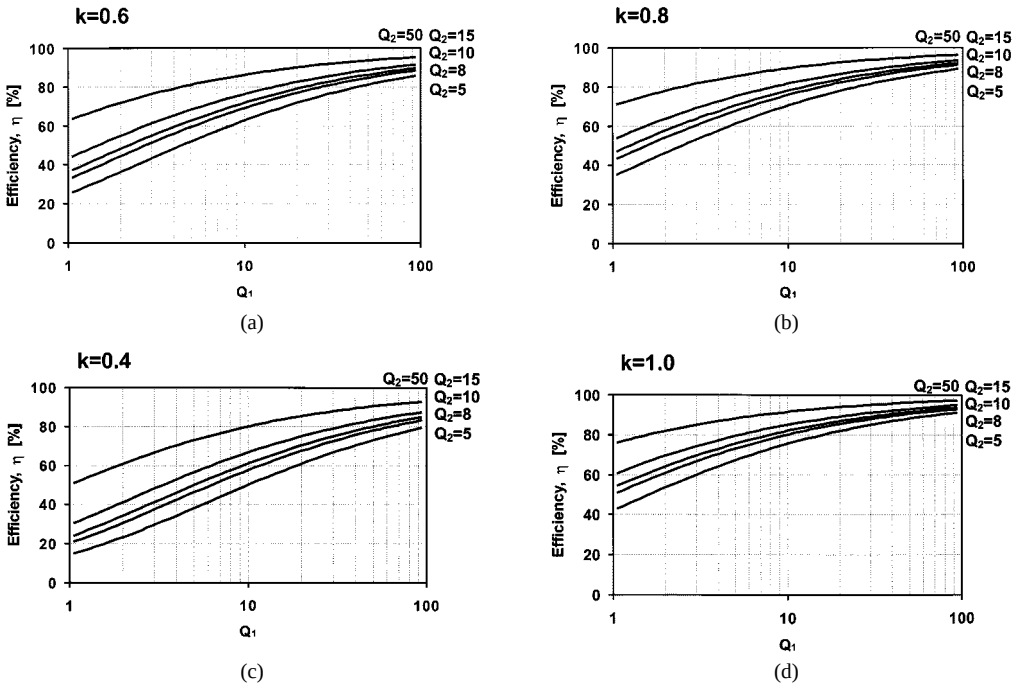


Fig. 11. Efficiency versus primary inductor Q_1, secondary inductor Q_2, and coupling factor k for a transformer with loss.

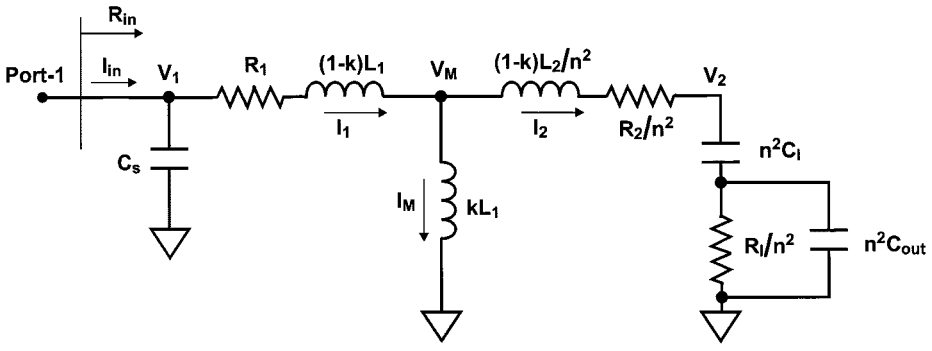


Fig. 12. Transformer equivalent T-model for analysis with load, tuning capacitors, and extra tuning capacitor in parallel to the load.

The new turn ratio n in this case will be

$$n \approx \sqrt{\frac{1}{1+A^2} \cdot \frac{E(Q_1/k^2+Q_2)}{\eta Q_1}}. \tag{29}$$

The efficiency η of this new setup is still given by (22). Note that plots of Fig. 11 are still valid since they are calculated in terms of quality factors. The maximum PER is achieved when C_l is very large. This maximum PER given by (26) is $(1+A^2)$ times larger than (24).[2]

In the design process, we start from a given transistor and a given power level that has to be delivered to the load. These two conditions determine the desired value of the PER E. Once this

[2]In practice, there is no need for C_l as the transformer dc isolation between the input and output ports allows us to short circuit C_l.

E is achieved, there is no point in increasing it beyond the required value, and we should maximize the efficiency η instead. As can be seen from (29), the addition of the parallel capacitor C_{out} makes it possible to use smaller turn ratio n for a desired E. Typically, a lower n results in a higher quality factor in magnetically coupled transformers, which translates to a higher efficiency, as can be seen from (22).

A capacitor C_s parallel to the transformer input completes this circuit. It tunes the reactive part of the transformer input impedance to the desired value appropriate to provide the required drain or collector impedance for the chosen class of the amplifier.[3]

Using the above analysis, we can compare the performance of a magnetically coupled transformer with an *LC*-based resonant impedance transformation discussed in Section II. Unlike the resonant *LC* matching circuit, in a magnetically coupled transformer the efficiency η does not depend on the PER E and, hence, does not drop for larger output power level, as can be seen from (11) and (22). The implicit assumption is that the quality factors do not change with larger n, which may not be correct as mentioned earlier. These equations shown graphically in Figs. 6 and 10 also show that for a PER above 15, the magnetically coupled transformer provides a higher efficiency η than the resonant matching for a given Q.

This difference in behavior arises from a fundamental difference between the *LC* resonant and magnetically coupled transformer matching, which can be understood using a simple model. In both approaches, in order to achieve a high PER, the input ac current I_{in} has to be larger than the output ac current I_{out} and the output ac voltage V_{out} has to be larger than the input ac voltage V_{in}, both approximately by $\sqrt{r}$.[4] In a resonant matching network, the loss is proportional to the product of I_{in} and V_{out}, which are both large. On the other hand, while in a magnetically coupled transformer, there are two loss components, namely, $I_{\text{in}} \cdot V_{\text{in}}$ and $I_{\text{out}} \cdot V_{\text{out}}$, each one is smaller than the single loss component in the case of a resonant matching by $\sqrt{r}$. Therefore, loosely speaking, the loss of the resonant matching circuit is larger by a factor of $\sqrt{r}/2$.

In a properly designed impedance-transformation network using magnetically coupled transformers, the reactance of the primary inductor ωL_1 is approximately the load resistance that should be seen by the active device, as seen in (20). Similarly, the reactance of output inductor , ωL_2 will be approximately the load resistance. Additionally, a negative reactance in series with the load is necessary to achieve the highest possible efficiency. This negative reactance can be generated by a combination of a series and a parallel capacitor, as shown in Fig. 12. These observations are particularly important for the DAT structure introduced in the following section.

The disadvantage of a magnetically coupled transformer is the low primary inductance necessary to achieve the highest efficiency. If spiral transformers on a silicon substrate were to be used, the small primary inductance results in extremely short metal lines. For instance, the necessary inductance to achieve an E of 50 into a 50-Ω load is approximately 80 pH at 2 GHz. Inter-winding these short primary metal lines with the multiturn secondary forces them to be very narrow. Unfortunately, this reduces the Q of both primary and secondary circuits, significantly. Noting the limitations of these two conventional impedance-transformation methods, we introduce an alternative solution, which does not suffer from these shortcomings.

[3]Although the tuning capacitor could be placed in series, biasing issues usually favor the parallel setting. However, the series arrangement has the advantage of resulting in yet smaller n.

[4]In a transformer, $\sqrt{r} \approx n$.

III. DAT

The analysis in these last two sections show that if we could increase the transformer turn ratio n while maintaining a constant Q, we could achieve a high efficiency for large PER, as suggested by (22) and (24). Unfortunately, the quality factor Q suffers if a large turn ratio is to be used for the reasons that will be discussed in Appendix C. Also (20) shows that the required impedance level at the input can become impractically small for large turn ratios because it is inversely proportional to n^2. These observations leave us no choice but to use lower turn ratios. In practice, the lowest loss can be achieved for a 1 : 1 ratio, which is also very appealing since high-Q coupled slab inductors discussed in Appendix C can be used to realize it.

While 1 : 1 transformers are desirable for the above reasons, it is obvious that we need more than one 1 : 1 transformer to obtain any impedance transformation. A high PER, can be achieved using N independent 1 : 1 transformers by connecting the secondary circuits in series, as shown in Fig. 13(a) and (b). In this arrangement, the ac voltages on the secondaries add, while the primaries can be driven at a low voltage by separate active devices. It should be noted that this configuration still has an impedance-transformation ratio N. Additionally, as there are N devices being power combined, the PER of such a (lossless) structure is N^2.

Unlike loop or spiral inductors, the two terminals of a slab inductor are not in close proximity of each other. This inherent property adds extra constraints to how they can be used. For example, if one is to make a parallel *LC* tank using a slab inductor, the parallel capacitor cannot be connected using regular wires, as the inductance and resistance of this wire will be comparable to that of the slab inductor. The absence of low-loss ground planes in silicon technologies exacerbates the situation and degrades the quality factor of a slab inductors, if they are configured in such a way that the return current conducts through the substrate.

A *double differential* drive can solve this problem in a power amplifier. A virtual ac ground is created in the middle of the slab inductor if differential push–pull transistors drive it. This virtual ac ground can be used as a dc feed for the power supply, making the impedance of the dc biasing networking inconsequential as far as the differential signal is concerned. The differential drive solves only half of the problem as the ground connection for the driving transistors are not going to be in close proximity with each other. It is necessary to form an ac ground by connecting the two transistor grounds to stop the ac current from flowing through the lossy ground line and, thus, induce extra loss. Again, a wire cannot be used to form this ac ground, as its inductance will be comparable to that of the slab inductor itself. This problem can be solved by a double-differential drive

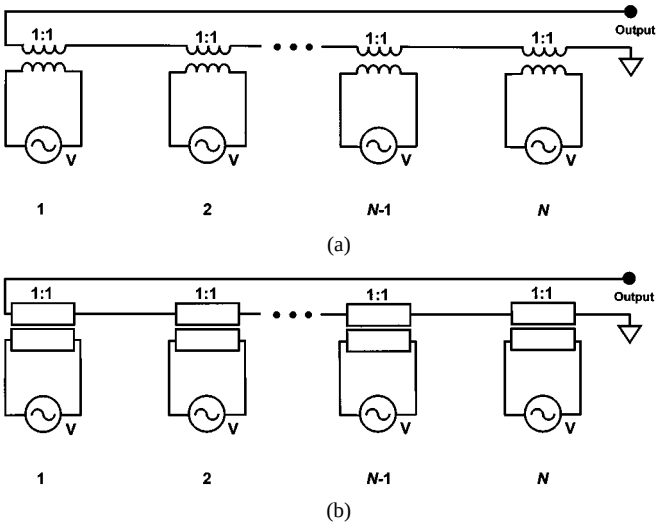


Fig. 13. (a) Fundamental building block of DAT. N independent power sources combined in series through N transformers with turn ratio $1:1$. (b) Same diagram using coupled slab inductors as the transformer.

shown in Fig. 14, where each driving transistor has an opposite phase to companion adjacent to it. In this case, the ac current flows through the adjacent transistors and hence an ac ground is created at their ground connections. Finally, to provide the same virtual ground for the two active devices at the ends of this combined structure, it can be wound to form a DAT, as depicted in Fig. 15(a) for slabs. Although this winding will reduce the Q of the inductors, due to the negative magnetic coupling between opposite sides of the polygon, this effect is significantly lower than winding each transformer individually as the dimension of the total structure is much larger. The schematic of Fig. 15(a) shows the central concept behind the DAT structure. In this configuration, the impedance-transformation and power-combining functions are achieved concurrently. Also all the dc currents are provided to the amplifier through virtual ac grounds, which makes the amplifier insensitive to the means used to supply the dc voltages (e.g., length of bonding wires).

The DAT combines the relatively high primary inductance of the *LC* matching networks, the PER-independent efficiency of a magnetically coupled transformer, and the high quality factor of slab inductors, while providing an effective means of power combining. In the DAT structure the loss is reduced because the voltages add on the secondary to combine power. Thus, the total ac current through the secondary inductor of the DAT is smaller than the current through the *LC* matching inductor by a factor of $\sqrt{r}$. Since the impedance of the DAT secondary is larger than the *LC* matching inductor by the same factor, the loss of the DAT is smaller than that of the *LC* match by approximately a factor of $\sqrt{r}$. Additionally, while large currents do flow through the magnetizing inductors of the primary circuits in a DAT, the low-loss slab inductors minimize the associated loss due to their higher Q.

As discussed earlier and shown in Fig. 9(a), the transformer's input shunt capacitor C_s is necessary for the transformer to present the proper impedance to the active device. As mentioned earlier, C_s cannot be placed in parallel with the slab inductors because of the physical distance between its terminals. However, placing capacitors between two adjacent ends of two slab inductors [see Fig. 15(b)] has exactly the same effect since the voltage across the capacitor will be identical to that of a capacitor in parallel with the slab. The output matching capacitor C_{out} can be simply placed in parallel to the load, as illustrated in Fig. 15(b). A representative drawing of this structure with eight NMOS transistors and four slab transformers is shown in Fig. 16.

A modified version of the transformer analysis described in Section II can be used to analyze the DAT. The new required primary inductance and the effective input admittance are given by

$$\omega L_1 = \frac{1}{(1+A^2)} \frac{A \cdot R_l}{N} \tag{30}$$

$$Y_{\text{in}} \approx \frac{1}{1+A^2} \cdot \frac{Q_1}{\frac{Q_1}{k^2}+Q_2} \cdot \left(\frac{N}{R_l} + j\frac{1}{\omega L_1}\right) \tag{31}$$

where N is the number of combined transistors. The new expressions for ωL_1 and Y_{in} in the presence of C_l and C_s can be derived using a similar derivation to that of Section II.

The definition of PER can be generalized to the case of a matching/transformation network with multiple input ports. In this scenario, it is natural to define the PER E as the ratio of the RF power delivered to the load with the network in place P_{trans} to the power delivered to load for one of the sinusoidal input voltage sources driving the load directly P_{one}. Based on this definition, the PER for the DAT can be calculated to be

$$E \equiv \frac{P_{\text{trans}}}{P_{\text{one}}} \approx (1+A^2) \cdot \eta \frac{N^2 Q_1}{\left(\frac{Q_1}{k^2}+Q_2\right)}. \tag{32}$$

Finally, the efficiency will be the same as the efficiency of a standard transformer matching circuit given by (22).

Several very important observations can be made about the DAT, when compared to conventional impedance-transformation networks.

1) The PER E of the DAT is proportional to the square of the number of transistors N, as shown by (32). This is comparable to the PER of a standard transformer matching circuit with a turn ratio n given by (26).
2) Comparing (27) and (30), it can be seen that the primary inductance L_1 will be N times larger in the DAT than the standard magnetically coupled transformers. This will allow the DAT to use values that are more practical for L_1 at the input ports.
3) In the DAT, N transistors generate the power and, therefore, each active device needs to deliver a smaller power to the passive structure. This difference manifests itself in (28) and (31), where the input conductance of each port in the DAT is N times smaller than the input of a standard magnetically coupled transformer.
4) Unlike *LC*-resonant matching networks, the loss mechanism of the DAT structure is independent of the PER to the first order. It is noteworthy that standard magnetically coupled transformers benefit from the same advantage.
5) The geometry of the DAT makes it possible to use $1:1$ slab transformers. In the DAT, we can make the primary

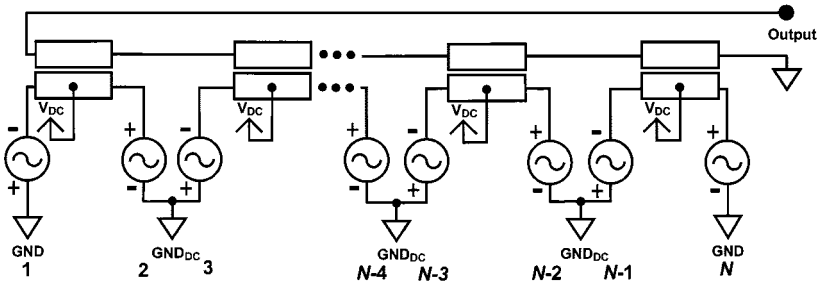
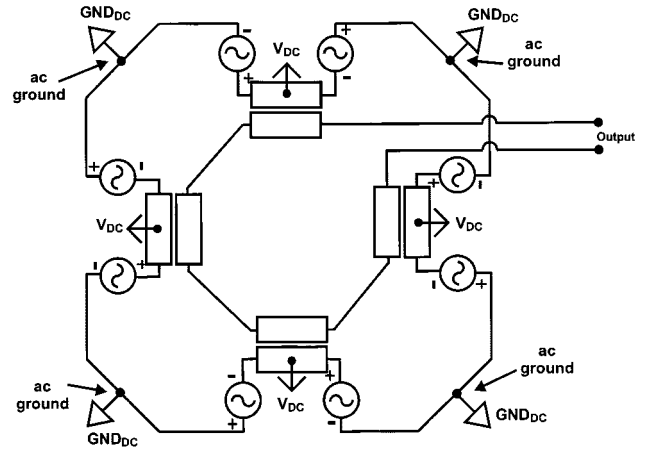
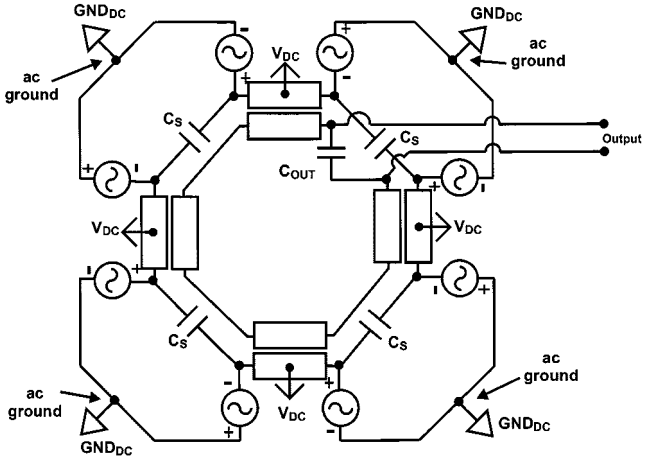


Fig. 14. N independent power sources combined in series through $N/2$ transformers in double-differential configuration with grounds shared between adjacent power sources, except for the first and last sources in the chain.



(a)



(b)

Fig. 15. (a) N independent power sources combined in series through $N/2$ transformers in double-differential configuration with grounds shared between every adjacent power sources using the circular geometry. (b) Same diagram with cross-connected drain tuning capacitors and output capacitor.

slab inductors wide to lower their series resistance. This reduction of loss in the primary is particularly important because large magnetizing currents flow in the primary circuits.

6) The two terminals of the slab inductors are not in close proximity of each other. The DAT uses a double-differential drive to be able to incorporate slab inductors into the design.
7) The distributed nature of the DAT can improve the thermal dissipation capability of the active devices up to a factor of N due to the more even distribution of the active device area across the chip.
8) The current in the secondary of the DAT is approximately N times smaller than in LC-resonant circuits, which allows narrower metal lines to be used on the secondary.

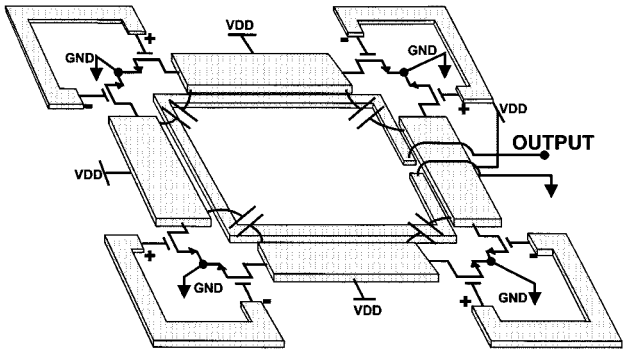


Fig. 16. Representative drawing of a complete DAT with 8 NMOS transistors.

Table I summarizes the performances of each one of the discussed power-combining, impedance-transformation and harmonic tuning techniques.

IV. A Design Example

In this section, we will demonstrate the design process of a 2-W power amplifier using 0.35-μm CMOS transistors with a drain breakdown voltage around 6 V. The passive parameters of this process are summarized in Table II.

For reliability, we should leave some margin for the maximum drain voltage to avoid junction breakdown. For this reason we limit the power supply to 2 V. To achieve 2 W output power into a 50-Ω load with a 2-V power supply, we need a PER higher than 50. For this design example, we have chosen a center frequency of 2.45 GHz.

Now, let us compare the performance of the three different methods of power enhancement discussed in Sections II and III. To obtain a PER of 50 using resonant impedance transformation (Section II-A), we need to use a three-stage network, as determined by Fig. 6. For this frequency and power level, the three inductors can be calculated using (15) to be 1.6, 0.35, and 0.075 nH. To obtain an estimate of the efficiency of the passive network, we can use ASITIC [22] to optimize these inductors, resulting in quality factors of 14, 10, and 3, respectively. The geometric mean of these quality factors can be used to approximate the efficiency of the passive network using Fig. 6. With a

TABLE I
COMPARISON OF CHARACTERISTICS OF SEVERAL LUMPED IMPEDANCE MATCHING AND POWER-COMBINING TECHNIQUES

	PER (E)	η	Power Combining	Drain Impedance	Lowest Inductor Impedance	Highest Inductor Impedance	Inductor Type	Harmonic Control
DAT	$\propto N^2$	Independent of E (22)	N	$\frac{R_{load}}{\sqrt{E}}$	$\frac{R_{load}}{\sqrt{E}}$	$\approx R_{load}$	Slab and single turn spiral	Classes A, B, C ,E/F$_x$, and inv. F
Transformer	$\propto n^2$	Independent of E (22)	1	$\frac{R_{load}}{E}$	$\frac{R_{load}}{E}$	$\approx R_{load}$	Multi turn spiral	Classes A, B, C ,E/F$_x$, and inv. F
Single LC-Resonant	$\left(\frac{R_{load}}{\omega L_p}\right)^2$	$1-\frac{\sqrt{E-1}}{Q_{ind}}$	1	$\frac{R_{load}}{E}$	$\frac{R_{load}}{\sqrt{E}}$	$\frac{R_{load}}{\sqrt{E}}$	Single turn spiral	Classes A, B, and C
Multi LC-Resonant	$\left(\frac{R_{load}}{\omega L_{p,1}}\right)^{2n}$	$\left(1-\frac{\sqrt{E^{\frac{1}{n}}-1}}{Q_{ind}}\right)^n$	1	$\frac{R_{load}}{E}$	$\frac{R_{load}}{E^{1-\frac{1}{2n}}}$	$\frac{R_{load}}{E^{\frac{1}{2n}}}$	Single turn spiral	Classes A, B, and C

where N is number of active devices combined in DAT, n is the turn ratio between primary and secondary circuits when referring to a transformer and the number of sections when referring to a multi-section resonant network, and E is PER.

TABLE II
PROCESS CHARACTERISTICS

Technology	0.35 μm BiCMOS
Oxide thickness to top metal	4.2 μm
Top metal sheet resistance	10 mΩ/□
Metal 2 sheet resistance	66 mΩ/□
Metal 1 sheet resistance	66 mΩ/□
Substrate conductivity	8 Ω.cm
Substrate thickness	400 μm
Top metal thickness	3 μm
Metal 2 thickness	0.5 μm
Metal 1 thichness	0.5 μm

mean Q of 7.5 the efficiency of the passive resonant matching network will be less than 50%. Even using a single *LC* section with an optimum[5] inductor Q of 15, Fig. 4 indicates that passive efficiency cannot exceed 52%. Note that this is the efficiency of the passive network alone assuming that ideal ac grounds can be provided and layout issues and parasitic components do not limit the performance. In practice, a resonator based passive network will have an even lower efficiency, for such high PER.

The second alternative is a standard coupled-inductor transformer. If we assume a typical inductor Q of eight and a coupling factor k of 0.6, we can obtain an efficiency of up to 68%, based on Fig. 10. Although this is higher than that of resonant network, it is extremely difficult (if not impossible) to layout a moderate-Q short and wide $1j\Omega$ (70 pH at 2.4 GHz) inductor[6] for the primary circuit and simultaneously inter-wind a secondary inductor with approximately $50j\Omega$ (3.3 nH at 2.4 GHz) and seven turns without reducing the quality factors. Due to the physical layout constraints, these standard transformers will have a very narrow metal width and/or a reactance significantly higher than $1j\Omega$. Due to these limitations, passive efficiency of these impedance-transformation networks will be much lower than the theoretically predicted upper limit of 68%.

Now, we can compare the *LC*-matching and coupled-inductor transformers with the DAT structure. Since the primary of the DAT consists of a slab inductor, it achieves a Q of more than 30 in this process technology. The secondary loop of the DAT structure has a Q of ten and coupling coefficient k of 0.6. The secondary parameters are comparable to a standard spiral transformer. Using (22), we predict a theoretical passive efficiency around 82%, for the DAT structure. As can be seen, The DAT achieves a higher passive efficiency than the resonant and standard transformer networks. Also, the double-differential drive of Fig. 15(b) generating multiple virtual grounds makes it possible to implement a DAT on a lossy silicon substrate without a significant reduction in this theoretically predicted passive efficiency due to biasing and ground connections.

To verify the feasibility of the DAT, the structure of Fig. 16 was simulated using Sonnet [24]. The primary slab inductors have a Q of 30, while the Q of the secondary loop is around eight. The electromagnetic simulations show a PER of 65. This translates to a maximum achievable output power of 2.5 W with a 2-V power supply. The simulated DAT passive efficiency was 70.5%. This in combination with the active device efficiency of 67.5% (operating in fully saturated class E/F_3 mode [25]) and a compressed gain of 10 dB, result in a PAE of 43%. The predicted drain efficiency is around 48%.

This truly fully integrated CMOS power amplifier was fabricated using 0.35-μm CMOS transistors. The measurement shows a PAE of 41% with a maximum output power of P_{out} of 1.9 W on a 2-V power supply, as shown in Fig. 17. The amplifier has a small signal gain of 14 dB and a compressed

[5]This is the best value that could be obtained using Sonnet [24] EM simulator for a spiral inductors in this process.

[6]The ASITIC optimized Q of this spiral inductor without the secondary is around three.

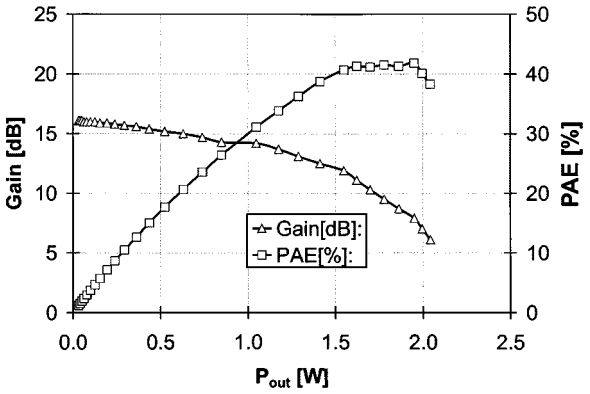


Fig. 17. Measured gain and PAE versus $P_{\rm out}$ of the DAT power amplifier when driving a differential load.

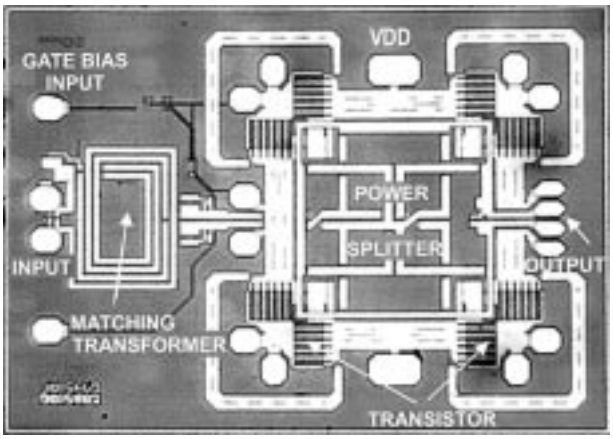


Fig. 18. Microphotograph of the measured DAT power amplifier.

gain of 8.7 dB at 1.9-W output power. Its drain efficiency is 48%. The input and output are both matched to 50 Ω, with an input reflection coefficient of −9 dB. The 3-dB bandwidth is 510 MHz centered at 2.44 GHz. All harmonics up to 20 GHz were more than 64 dBc below the fundamental. An on-chip balun allows for a single ended 50-Ω input. The same amplifier also provides a PAE of 31% with an output power of 2.2 W for an unbalanced 50-Ω load. The die size was 1.3×2.0 mm^2 and its microphotograph can be seen in Fig. 18.

Judging by the measured efficiency, we believe that every eight transistors are receiving fairly in-phase signals when the power amplifier is driving a symmetric differential load. On the other hand, the lower efficiency measured with unbalanced load is likely due to a phasing problem caused by an undesirable asymmetric feedback from the output.

A summary of these results can be seen in the Table III.

TABLE III
SUMMARY OF MEASURED AND SIMULATED AMPLIFIER PERFORMANCE

	Pout (W)	η (%)	PAE (%)	Gain (dB)	η active (%)	η passive (%)
Measured Differential	1.9	48	41	8.7	—	—
Measured Unbalanced	2.2	35	31	8.5	—	—
Simulated Unbalanced	2.5	48	43	10	67.5	70.5

V. CONCLUSION

A fundamental analysis of the loss mechanisms of the conventional on-chip impedance-transformation networks and their limitations are performed. We conclude the study with a description of the characteristics of the DAT. DAT is a new impedance-transformation and series power-combining architecture, which offers the advantages of *LC* and coupled-inductor matching simultaneously. Furthermore, it presents the advantage of power combining in series several amplifiers distributed across the chip without using additional components. This new concept combines in series several push–pull amplifiers efficiently by extensive use of virtual ac grounds and magnetic couplings.

APPENDIX A
RESONANT NETWORK EFFICIENCY COMPUTATION

To calculate the *LC* matching network efficiency η as a function of E and $Q_{\rm ind}$, we eliminate the terms r and η from the definition (10) using (5) and (6) and isolate the term $1/(1+R_{\rm load}/R_{lp})$ as follows:

$$E = r \cdot \eta = \frac{\left(1+\frac{R_{\rm load}}{R_{lp}}\right)^2 + Q_{\rm ind}^2 \left(\frac{R_{\rm load}}{R_{lp}}\right)^2}{\left(1+\frac{R_{\rm load}}{R_{lp}}\right)^2} \tag{A.1}$$

$$\frac{1}{1+\frac{R_{\rm load}}{R_{lp}}} = 1 - \frac{\sqrt{E-1}}{Q_{\rm ind}}.$$

This isolated term is η by (5)

$$\eta = \frac{1}{1+\frac{R_{\rm load}}{R_{lp}}} = 1 - \frac{\sqrt{E-1}}{Q_{\rm ind}}. \tag{A.2}$$

Equation (A.2) stands as E is approximately square of $R_{\rm load}/\omega L_p$ and $Q_{\rm ind}$ is $R_{lp}/\omega L_p$.

Substituting R_{lp} in the definition (4) using (A.1), we can find a solution for ωL_p, as shown by (12).

For the multisection case, we have

$$\begin{aligned}\eta &\equiv \frac{P_{\rm out}}{P_{\rm in}} \\ &= \eta_1\eta_2\eta_3\cdots\eta_n \\ &= \left(1-\frac{\sqrt{E_1-1}}{Q_{\rm ind}}\right)\left(1-\frac{\sqrt{E_2-1}}{Q_{\rm ind}}\right) \\ &\quad \cdots\left(1-\frac{\sqrt{E_n-1}}{Q_{\rm ind}}\right).\end{aligned} \tag{A.3}$$

If we assume that each individual E_k's are equal, we have

$$E = E_1E_2\cdots E_n \tag{A.4}$$

$$E_1 = E_2 = \cdots = E_n = E^{1/n} \tag{A.5}$$

and from the above, we obtain

$$\eta = \left(1 - \frac{\sqrt{E^{1/n} - 1}}{Q_{\text{ind}}}\right)^n. \tag{A.6}$$

The total efficiency of the network is the product of the efficiency of each stage. Simultaneously, if the total PER is E, the PER of each stage will be $E^{1/n}$. Analyzing the Fig. 5, we can calculate the inductor value for each stage in a similar way as in a single section network

$$\omega \cdot L_{p,1} = \frac{R_{lp,1}}{Q_{\text{ind}}} = \left(\frac{1}{\sqrt{E^{1/n} - 1}} - \frac{1}{Q_{\text{ind}}}\right) \cdot R_{\text{load}} \tag{A.7}$$

$$\omega \cdot L_{p,k} = \frac{R_{lp,k}}{Q_{\text{ind}}} = \left(\frac{1}{\sqrt{E^{1/n} - 1}} - \frac{1}{Q_{\text{ind}}}\right) \cdot R_{in,(k-1)}. \tag{A.8}$$

From (1), (A.1), and (A.2) we have

$$R_{in,k} = \frac{1 - \dfrac{\sqrt{E^{1/n} - 1}}{Q_{\text{ind}}}}{E^{1/n}} \cdot R_{in,(k-1)}. \tag{A.9}$$

From (A.7), (A.8) and (A.9) we have

$$\omega \cdot L_{p,k} = \left(\frac{1}{\sqrt{E^{1/n} - 1}} - \frac{1}{Q_{\text{ind}}}\right) \cdot \left(\frac{1 - \dfrac{\sqrt{E^{1/n} - 1}}{Q_{\text{ind}}}}{E^{1/n}}\right)^{k-1} R_{\text{load}}. \tag{A.10}$$

Appendix B
Transformer Efficiency Computation

The transformer efficiency η is the ratio of power P_{load} dissipated in the load resistance R_l and total power P_{total} dissipated in R_1, R_2, and R_l, shown in (B.1) at the bottom of this page, where

$$R_2' = \frac{R_2}{n^2} \quad R_l' = \frac{R_l}{n^2}. \tag{B.2}$$

To maximize η in the above expression, C_l should resonate L_2 at the frequency of interest, i.e.,

$$\frac{1}{\omega C_l} = \omega L_2. \tag{B.3}$$

This condition minimizes the current I_1 through R_1 and its dissipated power by resonating the inductors $(1-k)L_2/n^2$ and kL_1 with the capacitor C_l.

Assuming $L_1 \cong L_2/n^2$ and using (17) and (B.3), we can further simplify (B.1) to

$$\eta = \frac{R_l/n^2}{\dfrac{(\omega L_1/Q_2 + R_l/n^2)^2}{(\omega k L_1)^2} \cdot \dfrac{\omega L_1}{Q_1} + \dfrac{\omega L_1}{Q_2} + R_l/n^2} \tag{B.4}$$

which is obtained by dividing the equivalent load resistance R_l/n^2 by the sum of three equivalent resistances, which are R_2/n^2, R_l/n^2, and R_1 reduced by the ratio I_1/I_2.

Appendix C
Design of a Low Impedance Inductor

Inductors are essential blocks to design various forms of impedance-transformation networks and their properties can significantly affect the performance of such networks, as discussed earlier.

Spiral inductors [12], [15], [22] have been widely used in radio frequency integrated circuits. They can be single-turn or multiturn, as shown in Fig. 19. For a spiral inductor the negative magnetic coupling between the opposite sides of the polygon lowers its total equivalent inductance. However, this inductance reduction by negative mutual coupling does not occur when the distance between the opposite sides of the spiral is significantly larger than the mirror current penetration depth of the transmission line in the substrate.

In a single turn inductor with larger spacing between its opposite sides, the substrate (back plane) mirror current limits the inductance per metal length. Therefore, it behaves similarly to a microstrip transmission line of the same length. Also, the proximity of the opposite terminals of the inductor provides an alternative current path through the shunt-capacitors and the substrate that increases the loss.

$$\begin{aligned}
\eta &\equiv \frac{P_{\text{load}}}{P_{\text{total}}} \\
&= \frac{|I_2|^2 \cdot R_l'}{|I_1|^2 R_1 + |I_2|^2 (R_2' + R_l')} \\
&= \frac{|I_2|^2 \cdot R_l'}{|I_2 + I_M|^2 R_1 + |I_2|^2 (R_2' + R_l')} \\
&= \frac{|I_2|^2 \cdot R_l'}{|I_2|^2 \left(\dfrac{(R_2' + R_l')^2 + (\omega L_2/n^2 - 1/(n^2 \omega C_l))^2}{(k\omega L_1)^2}\right) R_1 + |I_2|^2 (R_2' + R_l')}
\end{aligned} \tag{B.1}$$

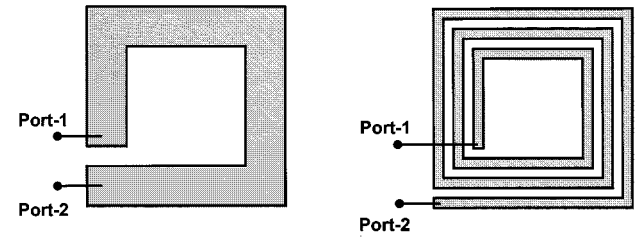


Fig. 19. One-turn planar spiral inductor and multiturn planar spiral inductor.

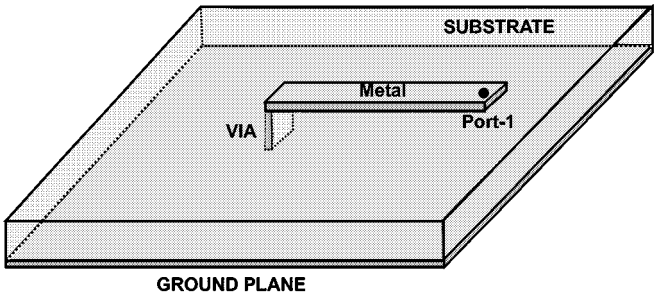


Fig. 20. Short transmission-line inductor with one terminal grounded on a dielectric substrate with backside ground plane.

If we use more than one turn to form a spiral inductor, the positive magnetic couplings between the conductors in the same side of the polygon enhance the total equivalent inductance.[7]

We can also build an inductor using a short transmission line with one of its terminals short-circuited to the ground, as in Fig. 20. Standard transmission-line analysis can be used to calculate the inductance and the Q of this inductor [18] as follows:

$$Z_{\text{ind}} = Z_o \cdot \tanh(\gamma \cdot l) \approx Z_o \left(\gamma \cdot l - \tfrac{1}{3}(\gamma \cdot l)^3\right) \qquad \text{(C.1)}$$

where Z_0 and γ are transmission line's characteristic impedance and complex propagation constant given by

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$
$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}. \qquad \text{(C.2)}$$

In which $R + j\omega L$ and $G + j\omega C$, are the series impedance and shunt admittance per unit length, respectively. Equation (C.1) shows that the inductance is proportional to the transmission-line characteristic impedance and its length. If the substrate has a low resistivity (e.g., in silicon), the loss terms in (C.2) will be large, which results in a relatively small inductor quality factor. In practice, it is very difficult to obtain analytical expressions for these loss components due to the nonuniformity of the conductor and substrate mirror current components, and one should resort to simulation methods [26].

For small lengths, the inductance of the microstrip transmission-line inductor is proportional to its length l, as shown in (C.1). Also, smaller line width w increases Z_0 and, hence, raise the inductance L. However, the dependence is weaker than linear due to the mutual coupling between parallel current components on the line. This behavior is shown in Fig. 21 where L is plotted versus w. This plot was obtained for a

[7]The multiturn spiral inductor also suffers from a larger parasitic capacitance between adjacent turns that lowers its self-resonant frequency.

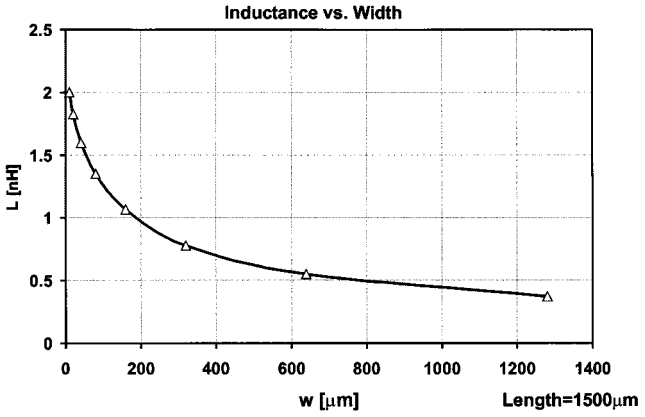


Fig. 21. Inductance of a transmission-line inductor versus metal width for constant metal length (1500 μm).

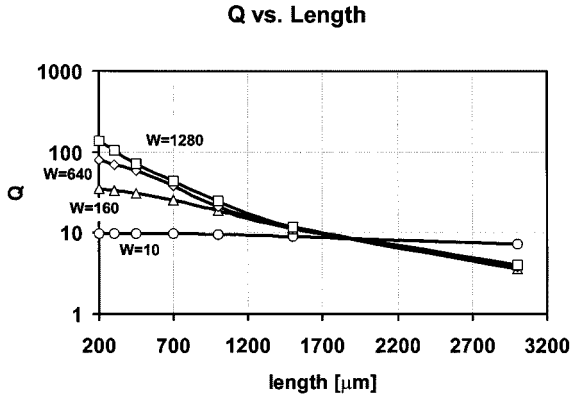


Fig. 22. Q of a transmission-line inductor versus metal length and metal width.

silicon process using a planar E/M simulator [24]. Fig. 22 shows plots of Q versus l for different values of w. The process characteristics used in the simulation can be seen in the Table III. Fig. 22 shows that series metal resistance, R, is the dominant loss factor for a narrow line (small w) and, hence, Q is approximately constant as a function of l. This is because both the series resistance and the inductance are proportional to l, thus their ratio Q remains constant, i.e.,

$$Q = \frac{\text{Im}(Z_{\text{ind}})}{\text{Re}(Z_{\text{ind}})} \propto \frac{\omega L \cdot l}{R \cdot l} = \frac{\omega L}{R}. \qquad \text{(C.3)}$$

On the other hand, the shunt elements G is the dominant loss factor for a wide line (large w). In this case, Q decreases almost quadratically with increasing l because both the series inductance and shunt-conductance scale with l, i.e.,

$$Q = \frac{\text{Im}(Y_{\text{ind}})}{\text{Re}(Y_{\text{ind}})} \propto \frac{1/\omega L \cdot l}{G \cdot l} = \frac{1}{\omega L G \cdot l^2}. \qquad \text{(C.4)}$$

Fig. 22 shows this behavior, where Q for $w = 10$ μm is almost constant with l, while it drops with l rapidly for $w = 1280$ μm. Consequently, we can conclude that microstrip inductor Q increases with increasing w when it is short and Q degrades with increasing w when the line is long, as illustrated in Fig. 22.

Based on this argument, we can find the w and l that maximize the Q for a desired inductance. This optimum Q is plotted

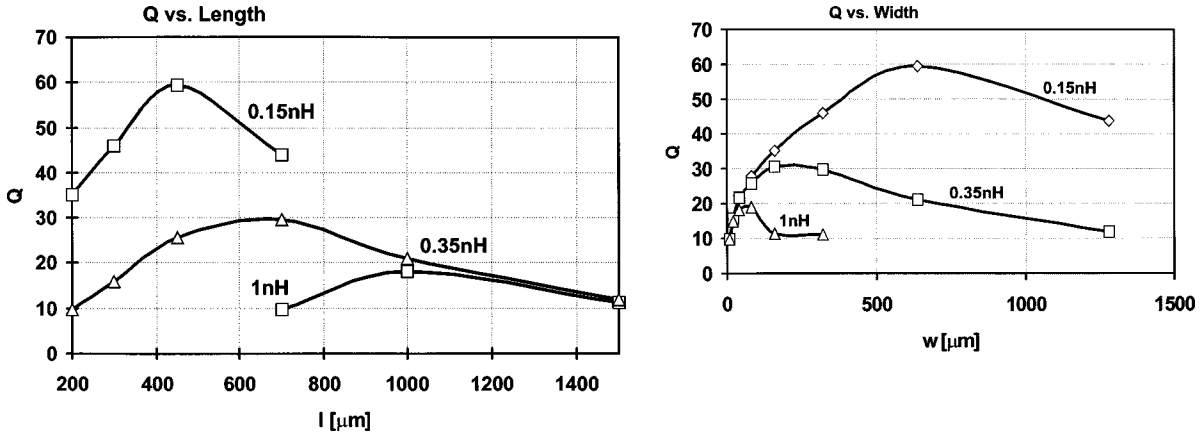


Fig. 23. Q of a transmission-line inductor versus metal length or metal width and inductance. In the first plot, for each metal length, the width, which provides the selected inductance, is chosen. In the second plot, for each metal width, the length, which provides the selected inductance, is chosen.

as functions of l and w in Fig. 23. The lower the inductance, the wider and shorter the optimum Q inductor. It should be noted that the optimum Q of a slab inductor with small L is much larger than typical quality factors of large spiral inductors, as shown in Fig. 23.

Based on these results, we can compare the three different types of inductor, namely, slab, single-turn, and multiturn inductors. The following guidelines can be used to obtain the best type of inductor in most practical applications.

If for a given L the reactance of a slab inductor ωL is much smaller than the transmission-line characteristic impedance Z_0, it will have a higher Q compared to spiral inductors. On the other hand, if the desired reactance of the inductor is larger or comparable to Z_0, multiturn spiral inductors should be used. One exception is when the transmission line is very low loss. In this case, a single ended high-Q inductor can be obtained using a transmission line shorter than quarter wavelength with one of its terminals grounded. In this case, the slab inductor is still preferred.

Another issue is that the terminals of a slab inductor are not adjacent to each other and this may preclude their use in certain applications. It is interesting to note that the slab inductors always outperform single loop inductor in terms of Q and, therefore, are always preferable unless two adjacent terminals are necessary.

ACKNOWLEDGMENT

The authors thank Conexant Systems for chip fabrication, particularly R. Magoon, F. In'tveld, J. Powell, A. Vo, and K. Moye. K. Potter, D. Ham, and H. Wu, all of the California Institute of Technology (Caltech), Pasadena, deserve special thanks for their assistance. The technical support for CAD tools from Agilent Technologies and Sonnet Software Inc., Liverpool, NY, are also appreciated.

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